REMARKS

Reconsideration of the above-identified application in view of the foregoing amendments and following remarks is respectfully requested.

A. Claim Status

Claims 1-20 are pending and were rejected under 35 U.S.C. § 103(a) as allegedly lacking patentable distinctiveness over U.S. Patent No. 6,972,635 to McCorquodale, et al. ("McCorquodale") in view of U.S. Patent No. 6,362,698 to Gupta ("Gupta") and further in view of U.S. Patent No. 6,268,778 to Mucke, et al. ("Mucke") and publication IEEE, ISSCC Vol. 12/2001 to Weldon, et al. ("Weldon"). [3/21/07 Office Action, p. 3].

B. Claims 1-20 are Patentably Distinct from the Cited References

Applicants respectfully traverse the 35 U.S.C. § 103(a) rejection of claims 1-20. McCorquodale, Gupta, Mucke, and Weldon, whether taken singly or in combination, do not teach, disclose or suggest each and every element of Applicants' independent claims 1 and 2. Accordingly, a rejection for obviousness is improper.

The Office Action contends that McCorquodale's frequency divider corresponds to Applicants' frequency divider in the external loop of the PLL system. [3/21/07 Office Action, p. 3]. However, McCorquodale is directed to an oscillator circuit which includes:

> ...first circuitry also fabricated on the substrate for converting the periodic signal into a high frequency digital output signal. [McCorquodale, Col. 13, lns. 29-31].
>
> and
>
> ...second circuitry also fabricated on the substrate for dividing the frequency of the digital output signal to the at least one lower desired application frequency ... [McCorquodale, Col. 13, lns. 36-39].

Referring to Fig. 8a of McCorquodale, the comparator may be regarded as a first circuitry whereas the D flip flop may be regarded as a second circuitry. As such, McCorquodale only discloses a single frequency divider (within a second circuitry) to factor the output signal from the VCO.

Applicants, on the other hand, describe an oscillating unit comprised of a PLL synthesizer which functions to raise the frequency of oscillation to a "frequency of n times a target frequency" and a frequency divider circuit "provided separately from the PLL synthesizer [for] dividing the output signal from the voltage controlled oscillator into 1/n frequency" as recited in amended claim 1. Consequently Applicants' oscillating unit has two frequency dividers whereas McCorquodale only discloses a single frequency divider. Furthermore, Applicants note that McCorquodale's Q and Qbar outputs are complementary signals in a digital circuit and do not necessarily have a phase difference of 180 degrees as contended by the Office Action. [3/21/07 Office Action, p. 3].

The Office Action then contends that Gupta discloses the PLL system as described by Applicants by referring specifically to Fig. 1 of Gupta. [3/21/07 Office Action, p. 3-4]. Conventional PLL circuits are limited in that they are used to control a VCO circuit by setting it at a frequency required for the operation of other circuits. However, in a conventional PLL circuit, a synthesizer does not control the oscillation circuit by setting the oscillation frequency at "n times a target frequency," thereby enabling incorporation of the required inductors and capacitors on the exiting IC as opposed to on an externally mounted circuit.

Applicants assert that it is not obvious for one of ordinary skill in the art to conceptualize the PLL circuit as disclosed by Applicants since to do so would require recognition and correlation of the following:

(a) Placement of a PLL synthesizer on the IC to control the oscillation frequency generated by an oscillation circuit by setting its frequency at n times a target frequency

and

(b) Utilization of a second frequency divider circuit on the same IC to factor the output signal from the VCO by 1/n.

Standard PLL circuits as disclosed in the prior art were developed solely to control the VCO oscillation frequency with there being no need to incorporate a frequency divider other than that used by the PLL circuit to divide the VCO frequency. Applicants assert that although the divider circuit of McCorquodale and the PLL circuit of Gupta are generally known, it would not be obvious to one of ordinary skill in the art at the time the invention was made to design a circuit which incorporates both (a) and (b) above. Accordingly, for at least the reasons discussed above, claim 1 is believed patentable over McCorquodale and Gupta, whether taken alone or in combination.

Applicants' claim 2 is directed to a PLL synthesizer comprising a first frequency divider and a second frequency divider other than the first divider to factor the output signal from a VCO circuit by 1/n. Thus, for at least reasons similar to those discussed above, claim 2 is also asserted to be in condition for allowance. Dependent claims 3-20 are also believed to define patentable subject matter for at least similar reasons.

In order to remedy the deficiencies in McCorquodale and Gupta, the Office Action attempts to rely on Mucke and Weldon. Mucke is cited by the Office Action as disclosing integrated type capacitance elements formed by MOSFETs whereas Weldon is cited as disclosing that the output from the divider circuit is sent to a mixer. [3/21/07 Office Action, p. 4]. However, both Mucke and Weldon fail to teach, disclose, or suggest each and every element of independent claims 1 and 2 as discussed above. That is, the ternary and quaternary

references fail to remedy the deficiencies of the primary and secondary references and, hence, a rejection for obviousness is improper. Accordingly, reconsideration and withdrawal of the rejections of claims 1-20 under 35 U.S.C. §103(a) is respectfully requested.

Applicants have chosen in the interest of expediting prosecution of this patent application to distinguish the cited documents from the pending claims as set forth above. These statements should not be regarded in any way as admissions that the cited documents are, in fact, prior art. Applicants have not specifically addressed the rejections of the dependent claims. Applicants respectfully submit that the independent claims, from which they depend, are in condition for allowance as set forth above. Accordingly, the dependent claims also are in condition for allowance. Applicants, however, reserve the right to address such rejections of the dependent claims in the future as appropriate.

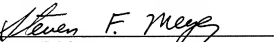
CONCLUSION

For the above-stated reasons, this application is respectfully asserted to be in condition for allowance. An early and favorable examination on the merits is requested. In the event that a telephone conference would facilitate the examination of this application in any way, the Examiner is invited to contact the undersigned at the number provided.

THE COMMISSIONER IS HEREBY AUTHORIZED TO CHARGE ANY ADDITIONAL FEES WHICH MAY BE REQUIRED FOR THE TIMELY CONSIDERATION OF THIS AMENDMENT UNDER 37 C.F.R. §§ 1.16 AND 1.17, OR CREDIT ANY OVERPAYMENT TO DEPOSIT ACCOUNT NO. 13-4500, ORDER NO. 5000-5247.

Respectfully submitted,
MORGAN & FINNEGAN, L.L.P.

Dated: July 23, 2007

By: 
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